Replacement Transmitter System for USCG Loran Recapitalization

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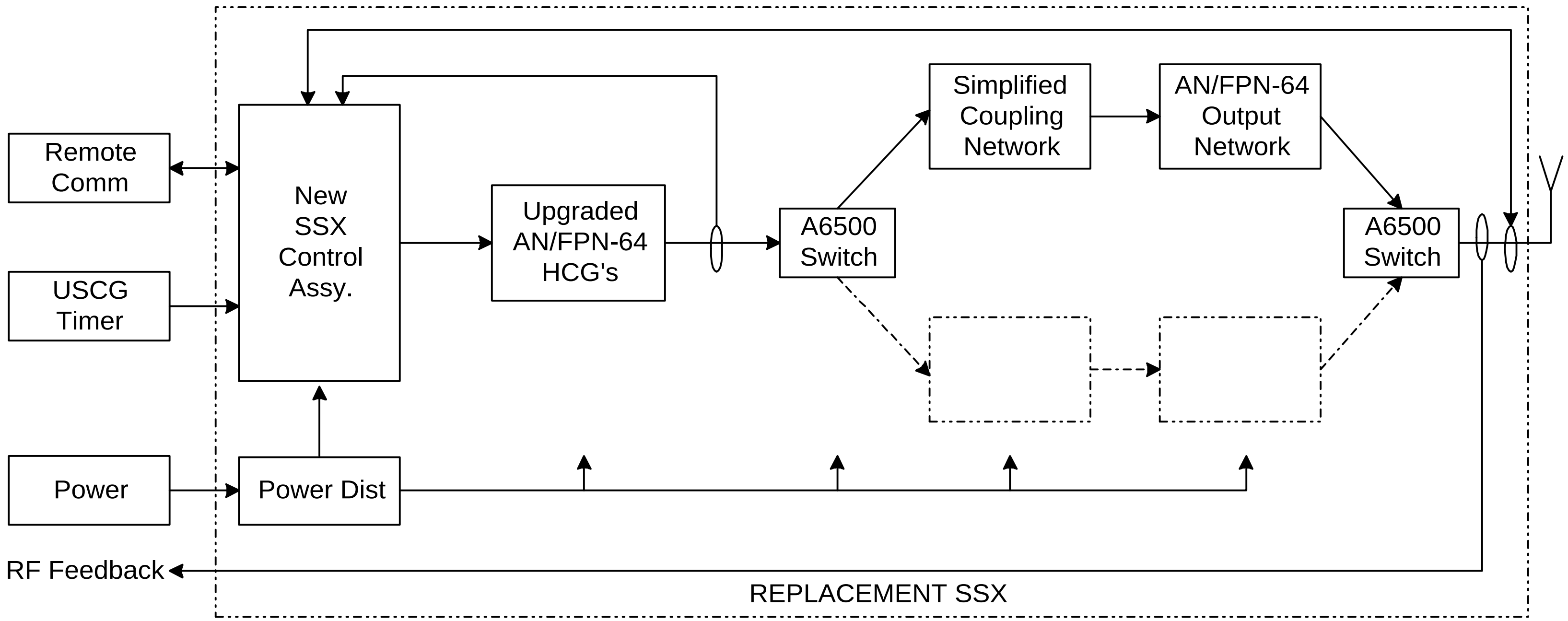
Requirements and Understanding

- USCG issues Performance Specification
  - Meet and exceed COMDTINST M16562
    - Controlling factors
    - Remote operability
    - Future requirements
    - Reduced operational cost
- Megapulse understands this to mean
  - TTX not supportable in the near term (NSITNT)
  - SSX control circuits NSITLT
  - TTX/SSX don’t support additional capabilities
  - Less bodies = Less $

General Design Strategy

- Goal:
  - The Megapulse technical response shall describe a replacement transmitter based on the following design goals:
    - Further increase individual HCG output power through improved components
    - Modernize Control Console assembly
    - Make the number of DHC's variable and assignments flexible
    - Future incorporation of IFM should have minimal impact on proposed architecture
    - Maximize commonality with exiting USCG assemblies

General Design Block Diagram



MP3611-A.VSD

Modernizations AN/FPN-64, A6500

- Increased Output Power/Higher Efficiency
  - Demonstrated in A6500
  - Modern components available with higher ratings open possibility further

Modernization AN/FPN-64, A6500

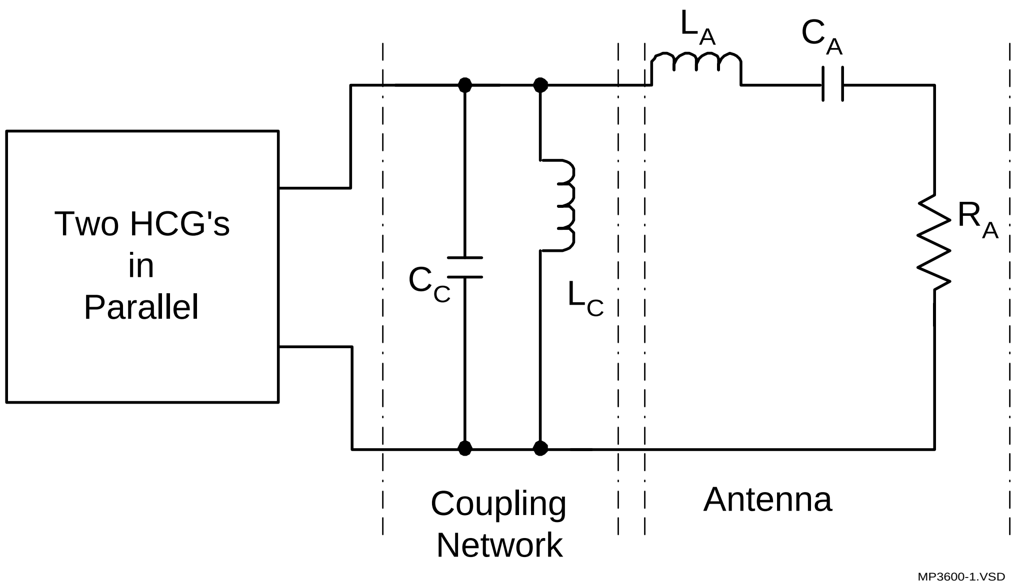
- Increasing Flexibility of DHCs
  - Original SSX prototype used 10 DHCs
  - Timing & amplitude was controlled by a PDP-11
- Idea was Revisited During "Dual Pulse" Tests
  - A 52 μsec time to peak Chayka pulse was generated using 4 DHCs
  - A 65μsec TTP Loran pulse was generated with 6 DHCs
  - Results published at Bonn DGON conf. Mar 2000
- DHCs that are Flexible and Reassigneable
  - ECD control will be more robust
  - Enhanced fail soft of HCG's
  - Allows for control of TTP

Design Verification Simulations &Tests

- Tests and Simulations were Performed to Verify Proposed Modernizations
  - Identify impact of increased voltages and currents (due to doubling the output power) on HCG components;
  - Ensure that Loran signal parameters (e.g. ECD, Tail Attenuation, etc) can be met with reduced number of HCG's.

High Power Test

- Schematic of Experimental Test Setup

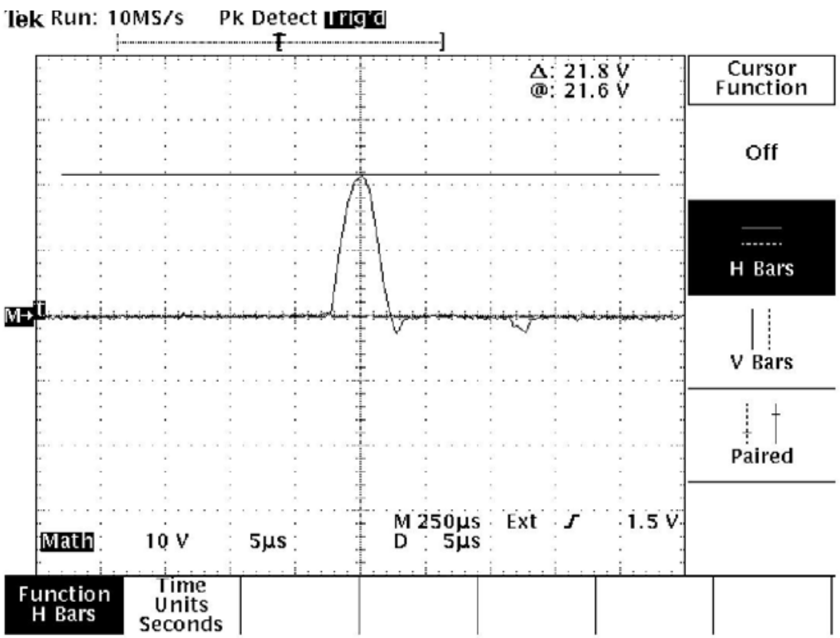


Experimental Test Setup

Experimental Test Setup (cont.)

Design Verification Simulation & Tests

- HCG Current into Coupling Network



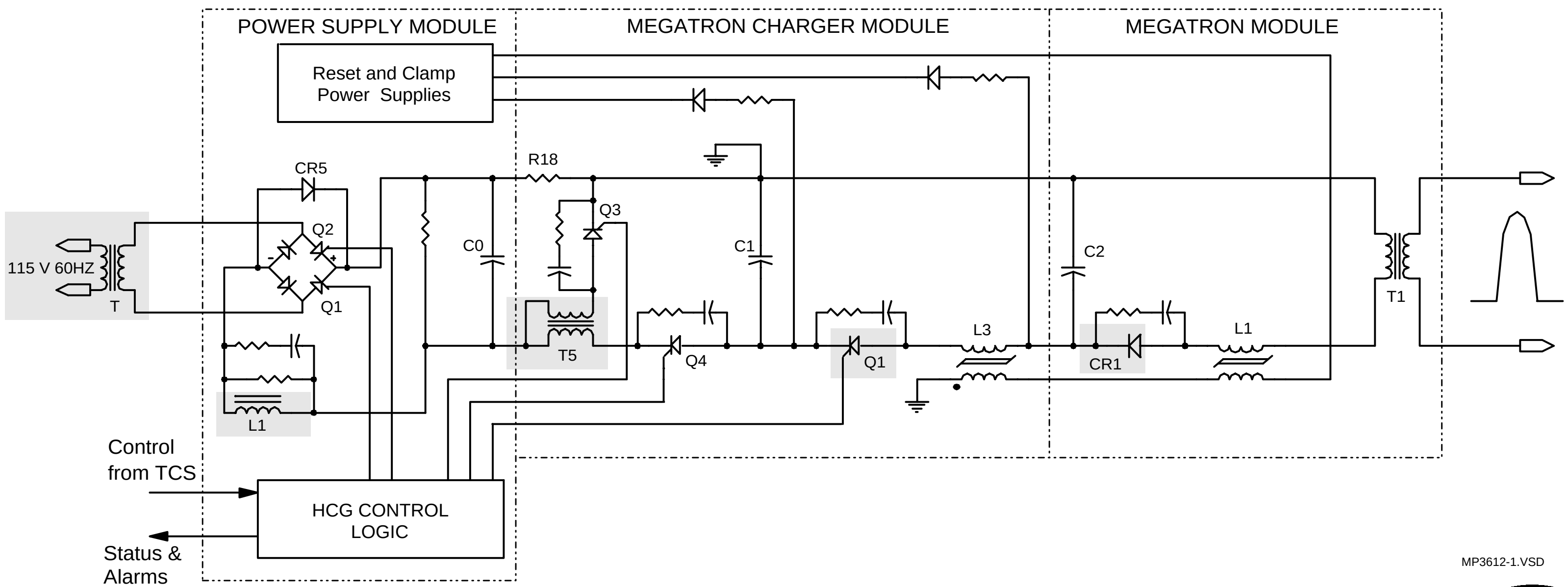
I_{HCG} = 872 Amps

MP3603-A.CDR

Design Verification Simulation & Tests

- Implications to Design of HCG

  (identified by shaded areas below)

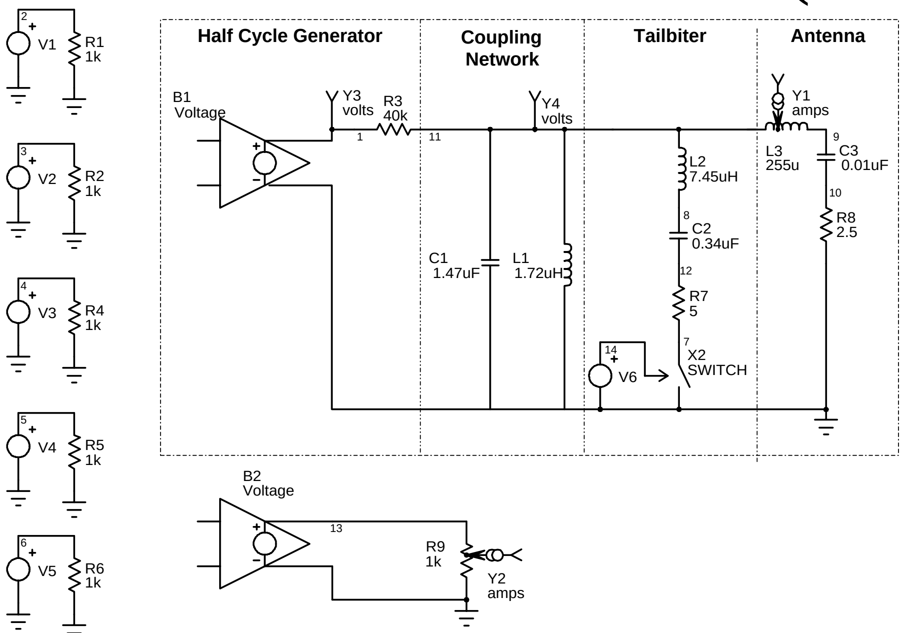


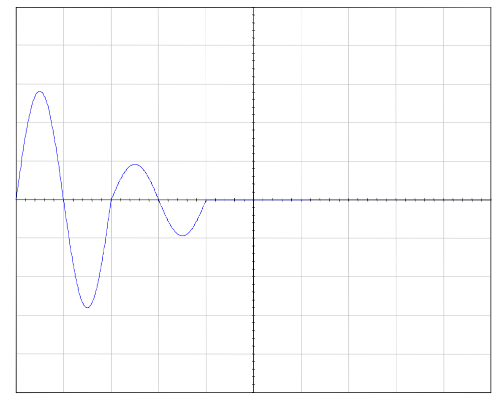
Design Verification Simulation & Tests

- IsSpice4 Software was used for Simulations
- 16 HCG Transmitter with 625ft TLM Antenna was Modeled
- Actual Cape Race Transmitter (32 HCG) Test Data was used as Reference to Validate Simulation Results
- Simulations Included:
  - Generations of Loran signals with full range of ECD's;
  - Verification of signal's tail attenuation (0.014A @ t>500sec);
  - Signal's spectrum compliance to specification

Design Verification Simulation & Tests

- Simulation Schematic (16 HCG-625ft TLM)

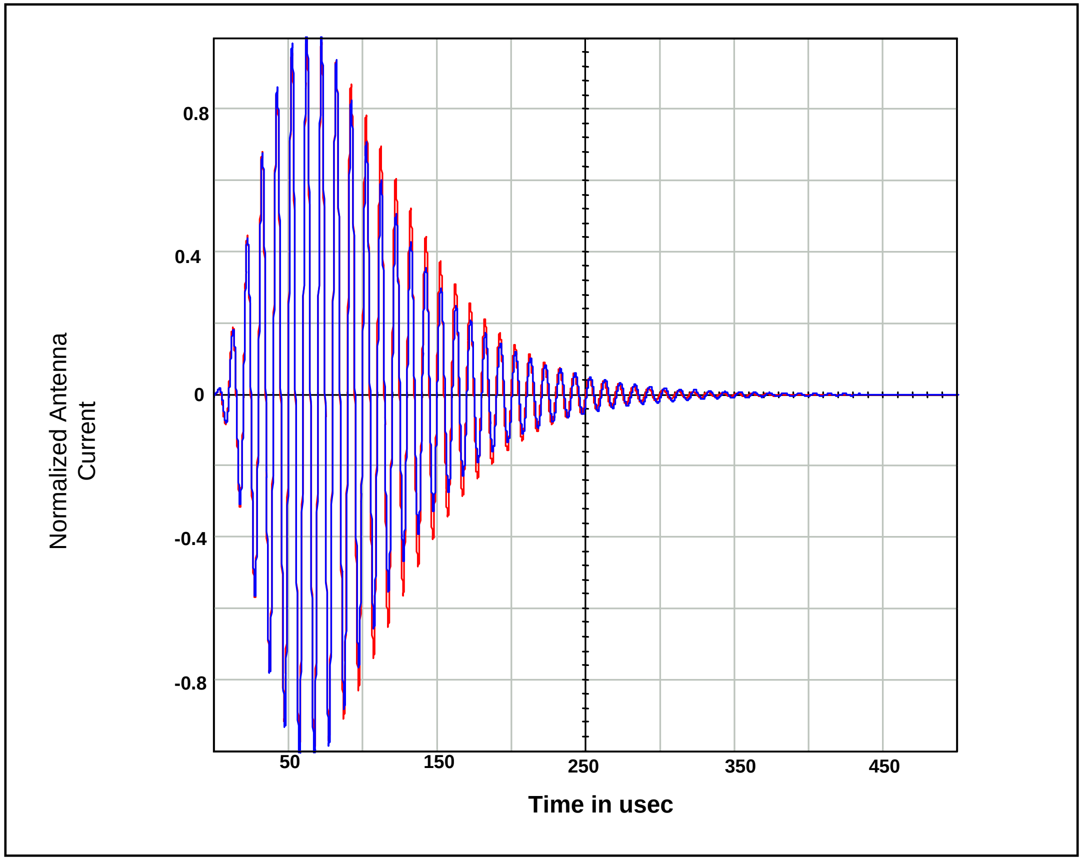




- V1 – 100kHz Sinewave Generator
- V2 – V5 – Generate 5µsec wide pulses at 5µsec intervals
- B1 – DHC Generator = V1*V2+V1*V3+V1*V4+V1*V5;
- B2 – Loran-C Signal Generator (per COMDTINST M16562.4A specification)

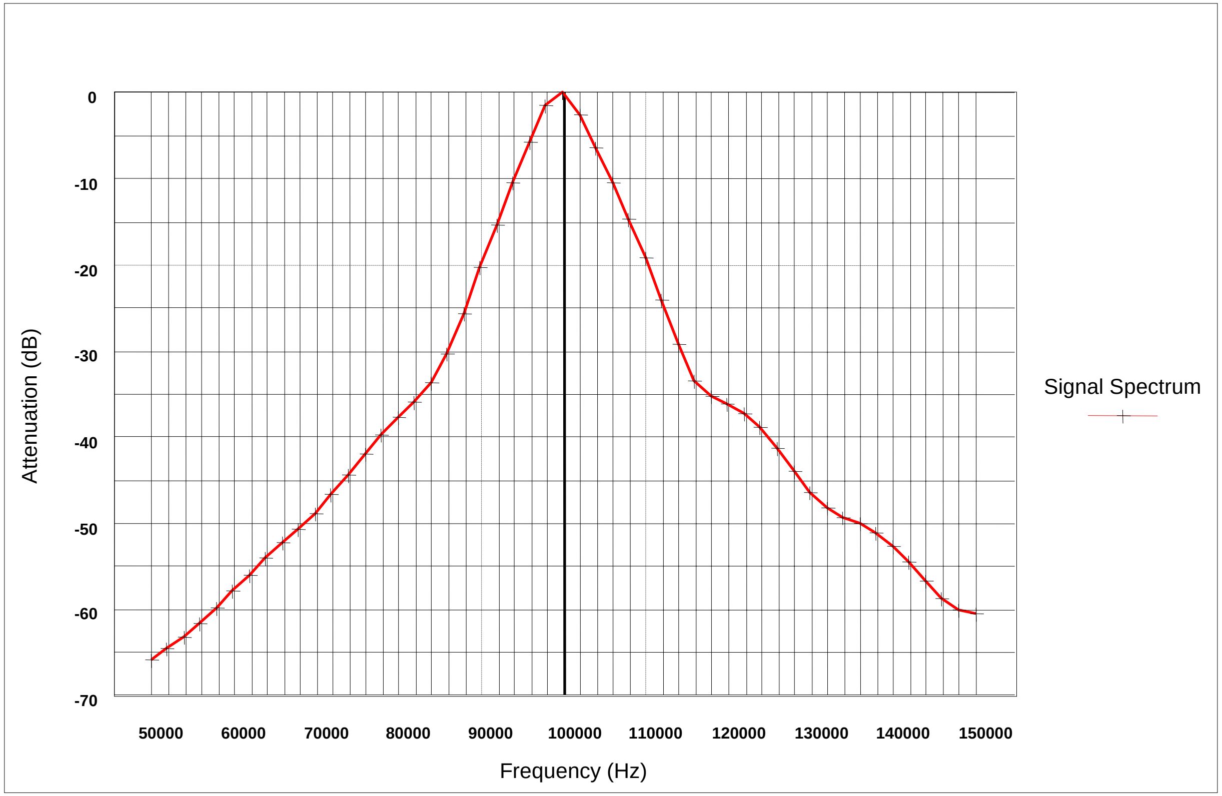
Design Verification Simulation & Tests

- Simulation Generated Loran Signal

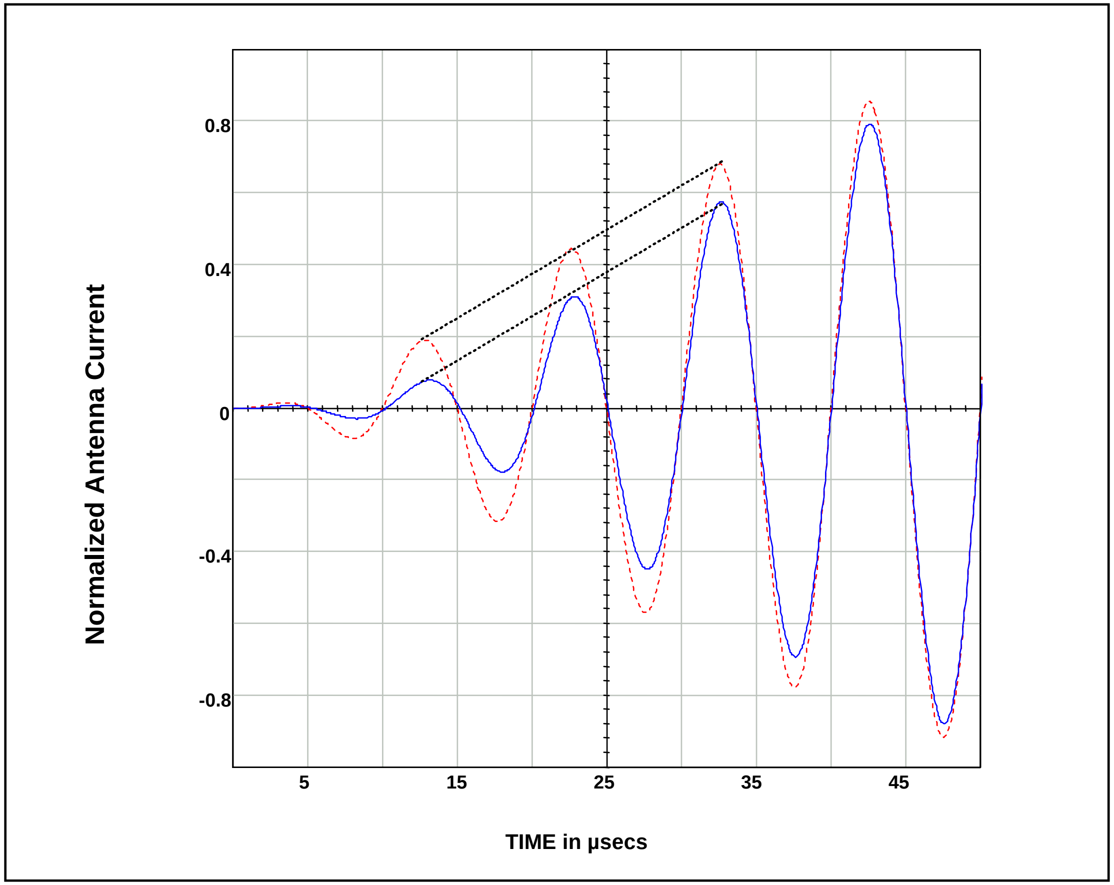


Design Verification Simulation & Tests

- Generated Loran signal spectrum



Design Verification Simulation & Tests



ECD = +5µsec

2 – 2 – 6 – 6

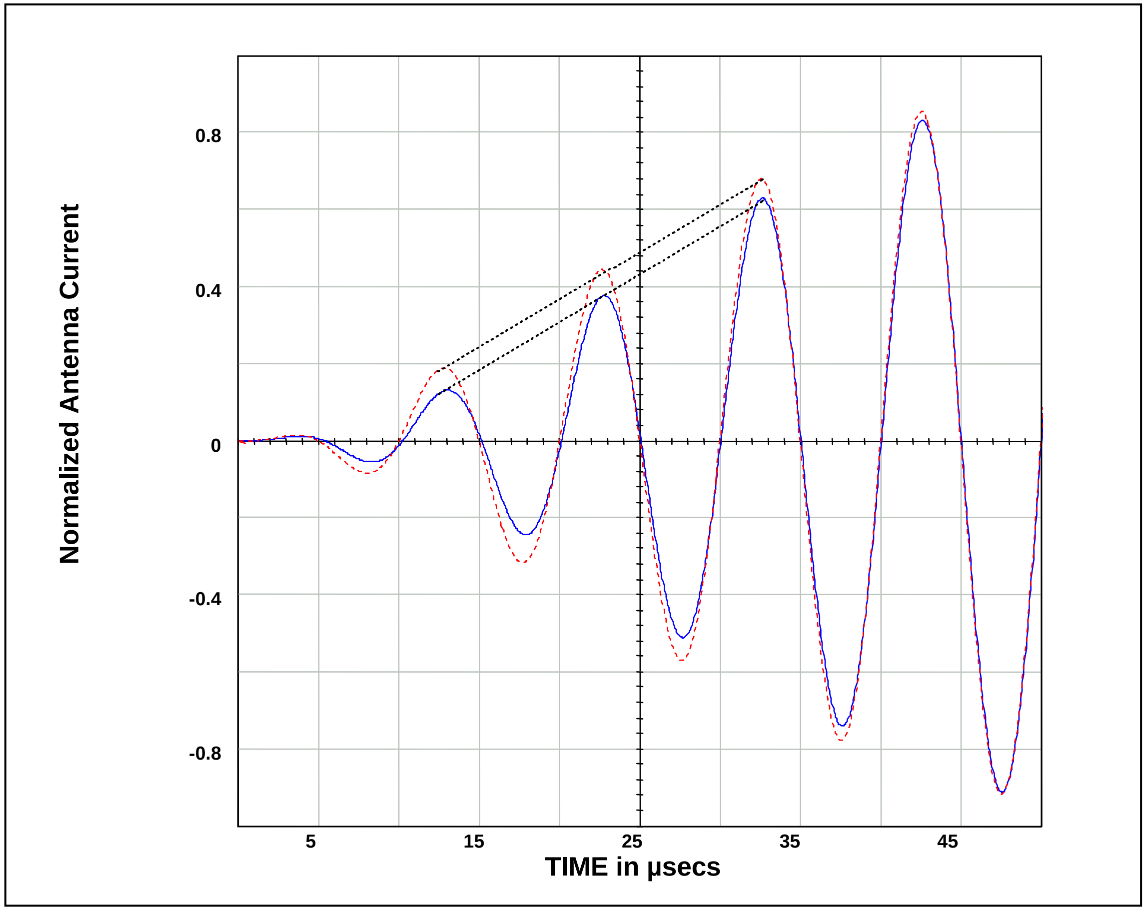
(2.2 – 2.1 – 6.1 – 6)

$(E_{SCR})_{MAX}$ = 1650*v*

$(E_{C1})_{MAX}$ = 1100*v*

$(I_A)_{MAX}$ = 665A

Design Verification Simulation & Tests



ECD = +2.5µsec

4 – 4 – 4 – 4

(4.2 – 4.1 – 4.03 – 4.03)

$(E_{SCR})_{MAX}$ = 1600*v*

$(E_{C1})_{MAX}$ = 1100*v*

$(I_A)_{MAX}$ = 665A

Design Verification Simulation & Tests

- Simulation Results
  - Full range of Loran signal ECD’s was generated. ECD “truth” table can be used as a reference in the design of Transmitter Control Assembly (TCA)
  - The same model will be used to generate HCG reassignment table for TCA, which will be used in case of HCG failure (soft fail concept)
  - Different values of Tailbiter components were analyzed with respect to tail attenuation requirements

TCS Design Philosophy

- Retain Existing System Partitioning
  - GFE Loran Timer and Remote Control
  - Control Console, XMTR and Power Distribution
- Retain Existing Functionality
  - Replace TOPCO, PATCO, SDA and Display Units
  - Auto “Fail-Over”/Redundancy
- Incorporate New Functionality
  - Support for Additional Drive Half Cycles
  - Dynamic Re-Assignment of HCGs
  - Real-Time Loran Signal Quality Analysis (SQA)
  - Interpulse Modulation (Supernumerary)
- Allow for Future Capabilities
  - Intrapulse Frequency Modulation (IFM)

Functional Decomposition - Summary

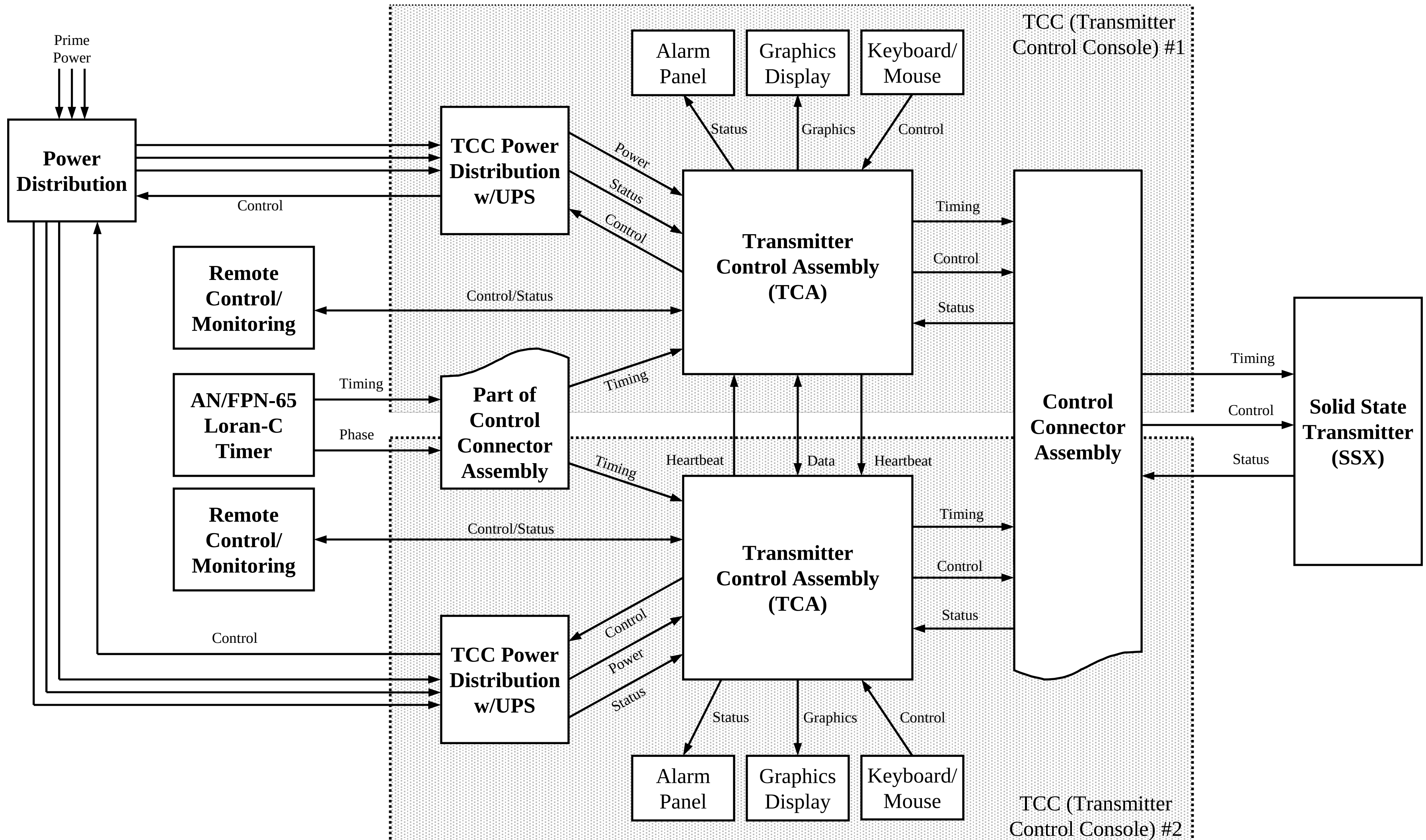
TCS Functional Decomposition

- **User / Maintainer / Remote Interface**
  - Operator/Maintainer Screens
  - Display/Keyboard/Mouse
  - Alarm Panel Control
  - Event/Data Logging
  - Remote Control and Data Logging (RS-232)
  - Redundancy Management
  - UPS Monitoring
- **Loran Timer/HCG Signal Processor**
  - Loran Timer Signal Conditioning
  - Timing Signal Generation
  - MTS Serial Stream Generation
  - DHC Feedback Processing
  - Tailbiter Trigger Generation
  - A/B Rate Failsafe Blanking
  - Tailbiter Monitor Synchronization
- **General XMTR Commands/Status/Faults**
  - RF Switch Control /Monitoring
  - Antenna Tuning Control /Status
  - HCG Fault Monitoring
  - Tailbiter Fault Monitoring
  - Output Network Fault Monitoring
  - Coupling Network Fault Monitoring
  - PPD Commands/Status
- **Embedded LORDAC Functionality**
  - Antenna Tuning Support
  - ECD Calculation
  - Loran SQA

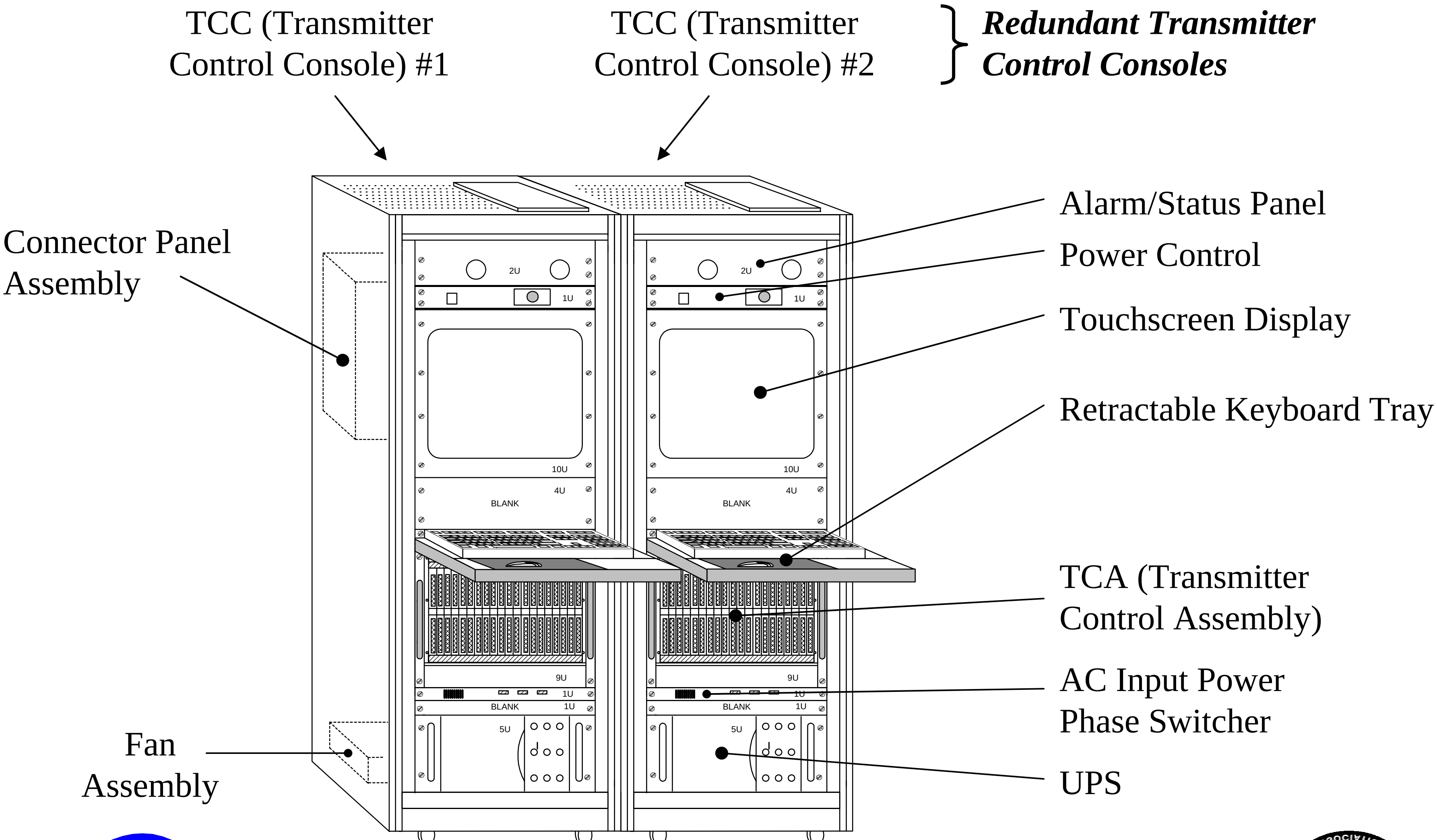
TCS Design Approach

- Redundant Design
- Commercial Off-The-Shelf (COTS) to Reduce Schedule/Technical Risk
- Card Based CPU for Reliability/Maintainability
- Hardware Independent C/C++ Software
- Graphics Display, Keyboard and Pointing Device Support
- Rear Panel Signal I/O with MS Style Connectors
- 19” Rack Mounting with Forced Air Cooling

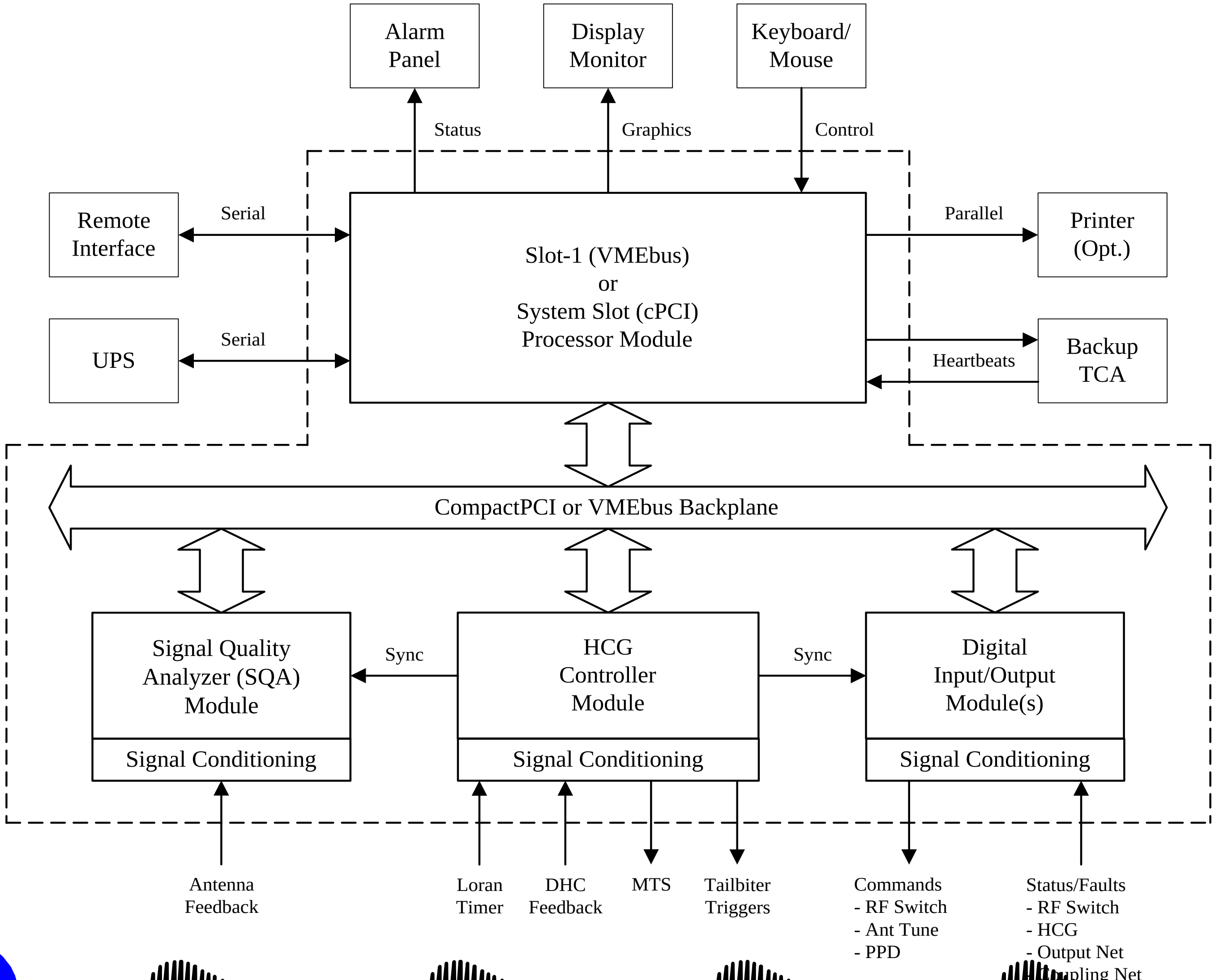
TCS Block Diagram



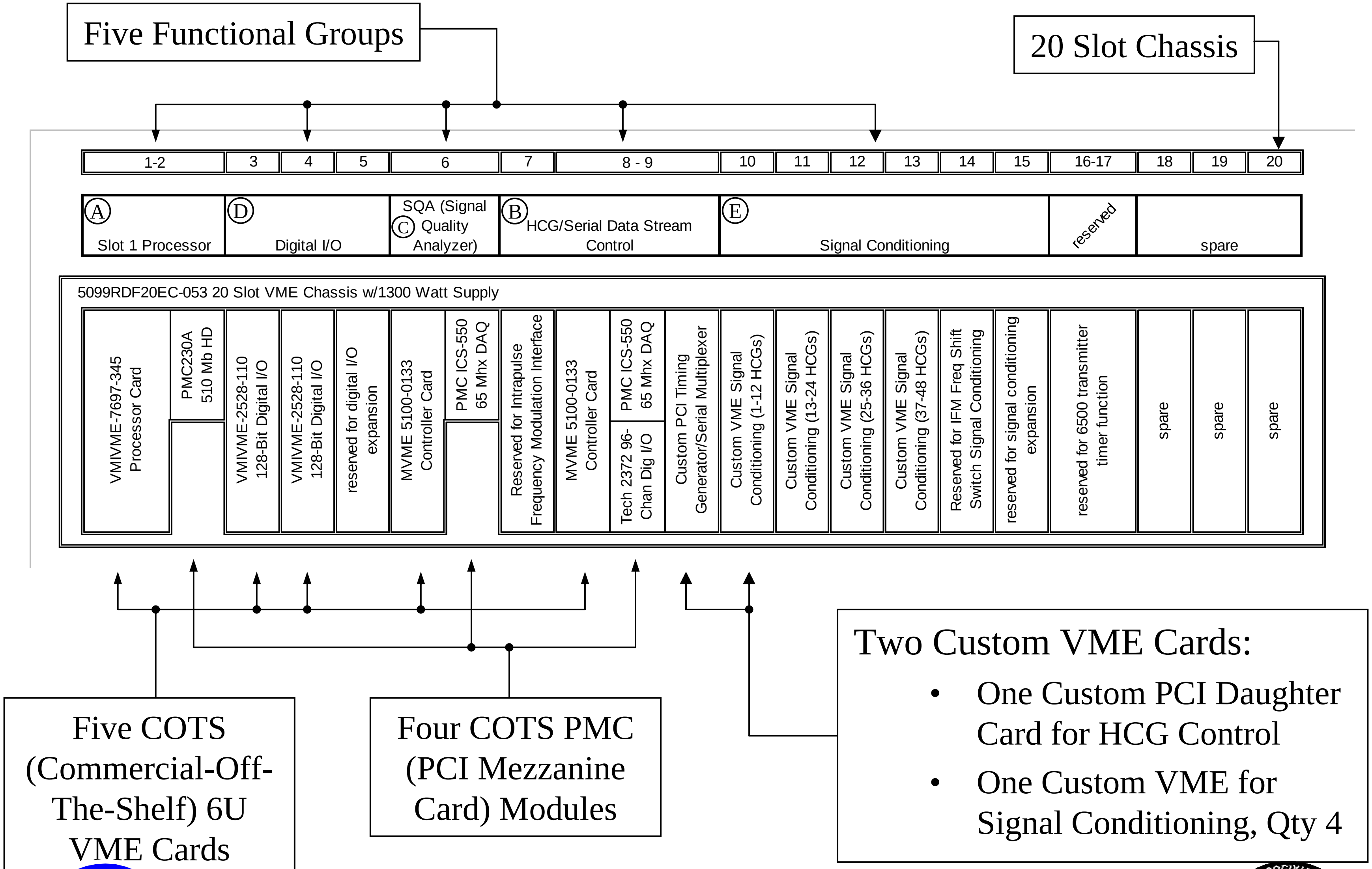
Transmitter Control Subsystem



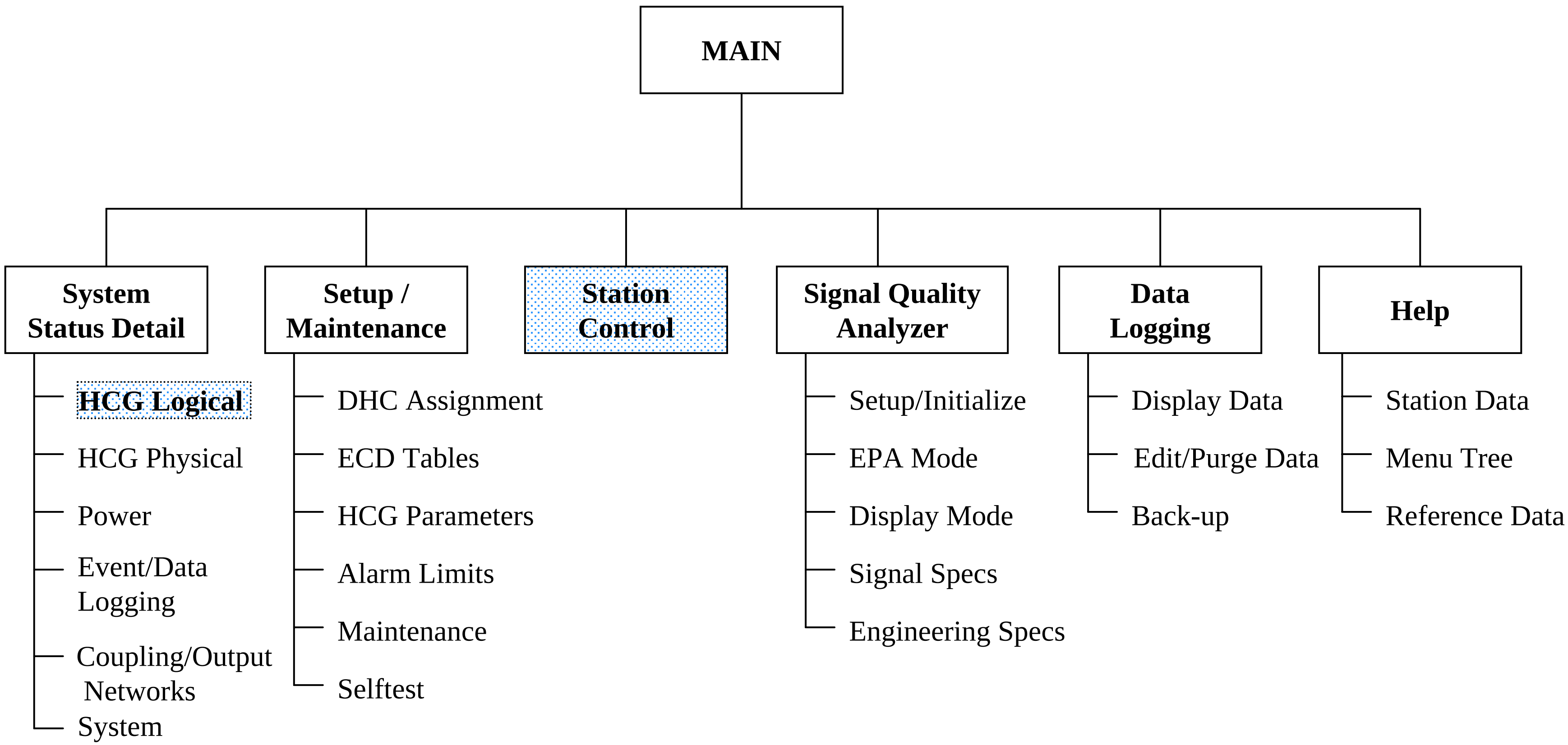
TCA Block Diagram



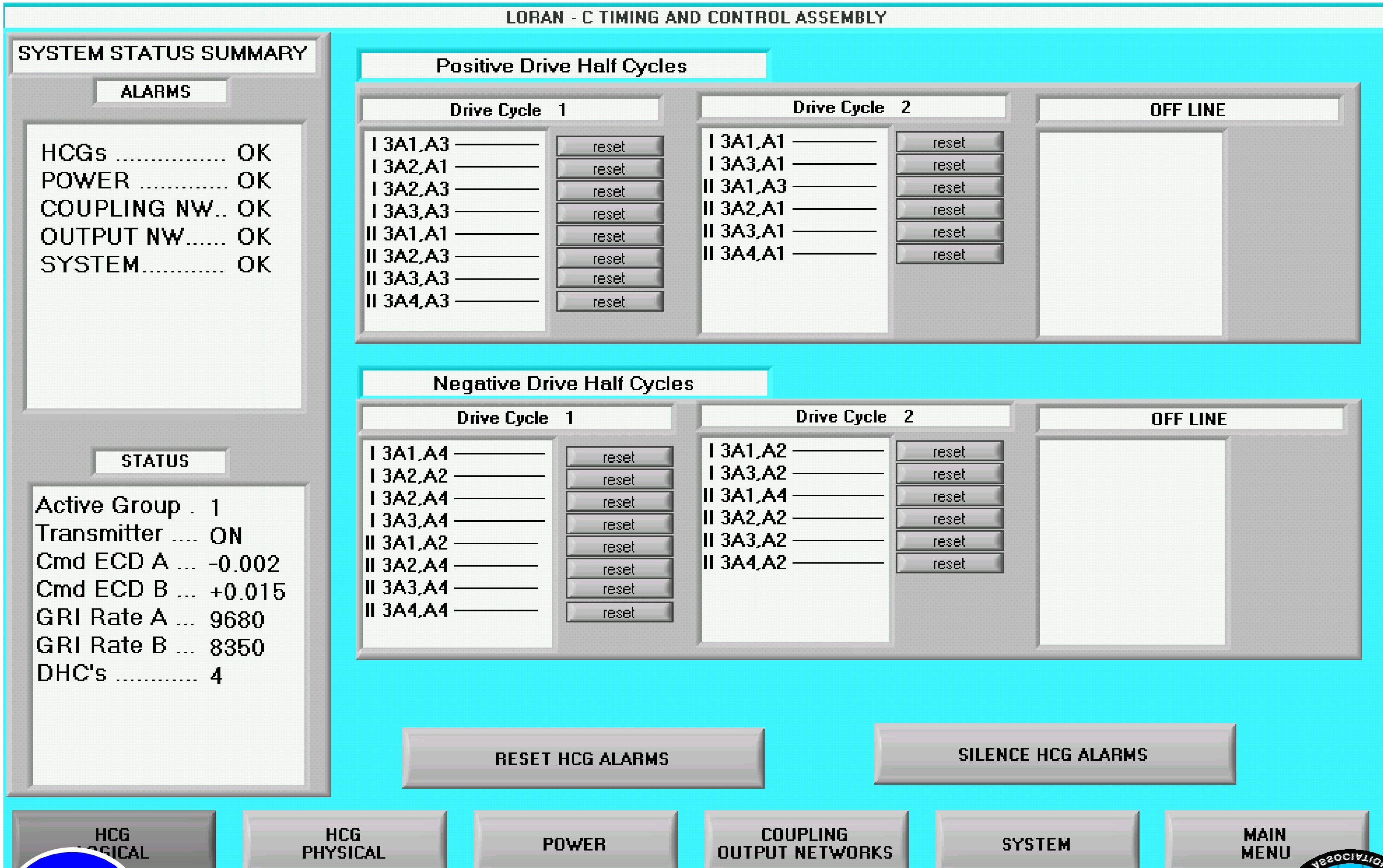
TCA - VME Chassis



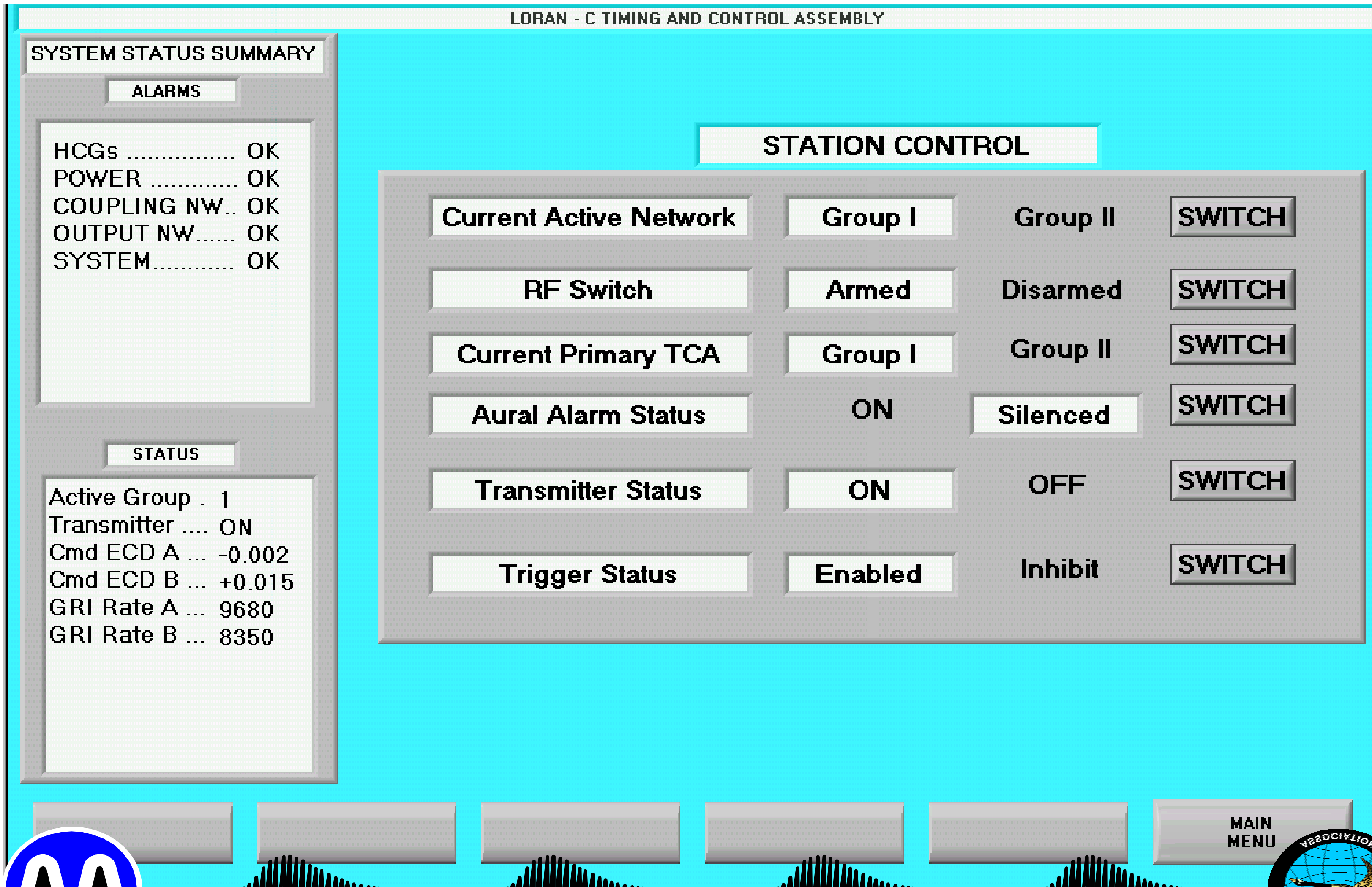
User Interface Menu Tree



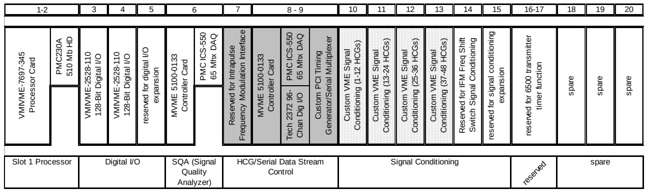
HCG Alarm/Status Screen



Station Control Screen



HCG/SDSC Methodology

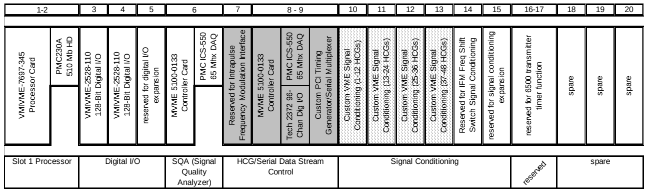


- HCG Control Methodology
  - Current System Design Analyzed
    - Similar Approach for Control of HCGs Chosen
      - Reduce development
      - Minimize risk
      - Improve maintainability
  - Timing Analyzed for Support of:
    - Utilization of Additional Half Cycles to Improve Transmitter Efficiency

HCG Control Similar to Existing System Control Methodology

HCG/SDSC Functions

- Main HCG/SDSC Functions are as Follows:

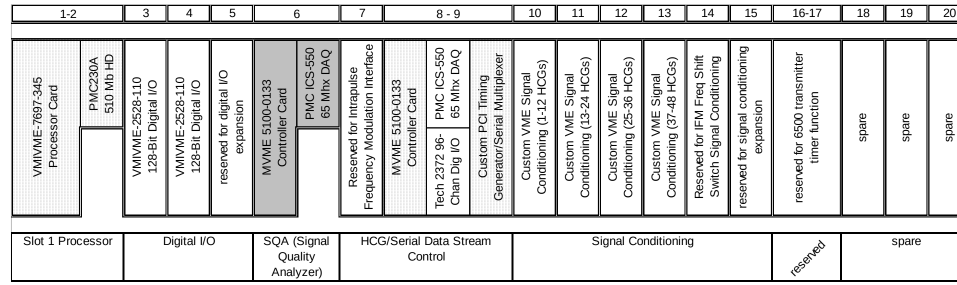


  - **Failsafe Blanking**
  - **Timing and Triggering for the TCA Based on USCG Timer Signals**
  - **Polarity Control for Loran Pulse Phase Coding Based on USCG Set and Reset Pulses**
  - **High Speed Sampling of HCG Feedback**
    - **Adjust HCG Amplitude and Trigger Timing Based on Feedback Analysis**
  - **Generate Four (4) Serial Data Streams, One for Each Group of HCGs**
  - **Allocate HCGs to Required Drive Cycle Based on Programmed System Settings**
  - **Generate Transmitter Tailbiter Triggers**
  - **Future Generation of FSS (Frequency Shift Switches) Control Signals for IFM Based on Coast Guard Control**

HCG/Serial Controller Software

- Functions Performed
  - Initializes MTS Data, Tailbiter Trigger and Frequency Shift Switch Control Signal Data Buffers
  - Monitors DHC Feedback Signal from DAQ HW Module
  - Computes DHC Magnitude and Zero Crossing Values
  - Based on These Computed Values, Adjusts MTS Amplitude and Delay Values as Required
  - Loops Once per LORAN Pulse
  - Provides All Data for Use by Main Processor
  - Performs Self Health Monitoring
  - Inhibits Signal Outputs if in Backup Mode

Signal Quality Analyzer (SQA) Group



- The SQA Group Consists of the Following:
  - One (1) Processor Card [MVME5100-013]
  - One (1) 65 Mhz DAQ (Data Acquisition) PMC Card [ICS-550]
- Main SQA Functions are as follows:
  - High Speed Sampling of Antenna Feedback
    - Adjust Antenna Tuning Based on Feedback Analysis
    - The Functional Capability of the PC-LORDAC Test capability includes both Signal Specification tests and Engineering Specification tests
  - Future Analysis of Output Waveform for Intrapulse Frequency Modulation

Summary

- Cost Effective
- Higher Efficiency
- Managed Risk
- Flexible Control Architecture
- Familiar Assemblies
- Enhanced Maintainability and Operability